Amendment dated July 25, 2003

Reply to Office Action of March 25, 2003

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously amended): A voltage generating/transferring circuit comprising:

a boost unit group including a plurality of boost units series-connected between input and output nodes;

a first transistor connected between the input node and a node for receiving a first voltage; and

a first capacitor having one end which is connected to the output node, and another end which receives a first oscillation signal,

wherein each boost unit has input and output portions, a second transistor having a gate and a drain connected to the input portion and a source connected to the output portion, and a second capacitor in each boost unit connected to the input portion, and a gate of said first transistor is connected to the input portion of one of the boost units.

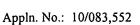
Claim 2 (original): A voltage generating/transferring circuit according to claim 1, wherein said boost unit group includes not less than three boost units.

Claim 3 (previously amended): A voltage generating/transferring circuit according to claim 1, further comprising:

a third transistor which has a gate connected to the output node, and transfers a third voltage,

wherein a second voltage of the gate of said third transistor is equal to, or larger than a sum of the third voltage and a threshold voltage of said third transistor.

Claim 4 (previously amended): A voltage generating/transferring circuit according to claim 1, wherein a second oscillation signal is input to an even-numbered boost unit from the input node, a third oscillation signal is input to an odd-numbered boost unit from the input node, and the second and the third oscillation signals have opposite phases or different timings.



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Claim 10 (previously added): A voltage generating/transferring circuit according to claim 1, further comprising:

a third transistor which has a gate connected to the output node, and transfers a third voltage,

wherein a second voltage of the gate of said third transistor is equal to, or larger than a sum of the third voltage and a threshold voltage of said third transistor in transferring the third voltage.

Claim 11 (previously amended): A voltage generating/transferring circuit comprising:

a boost unit group including a plurality of boost units series-connected between input and output nodes;

a first transistor connected between the input node and a node for receiving a first voltage; and

a first capacitor having one end which is connected to the output node, and another end which receives a first oscillation signal,

wherein each of the boost units has input and output portions, a second transistor having a gate and a drain connected to the input portion and a source connected to the output portion, and a second capacitor in each of the boost units connected to the input portion, a charge moves between the output portion of one of the boost units and the input portion of another of the boost units, and a gate of said first transistor is connected to the input portion of one of the boost units.

Claim 12 (previously added): A voltage generating/transferring circuit according to claim 11, wherein said boost unit group includes not less than three boost units.

Claim 13 (previously added): A voltage generating/transferring circuit according to claim 11, further comprising:

a third transistor which has a gate connected to the output node, and transfers a third voltage,

wherein a second voltage of the gate of said third transistor is equal to, or larger than a sum of the third voltage and a threshold voltage of said third transistor.

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Claim 14 (previously amended): A voltage generating/transferring circuit according to claim 11, wherein a second oscillation signal is input to an even-numbered boost unit from the input node, a third oscillation signal is input to an odd-numbered boost unit from the input node, and the second and the third oscillation signals have opposite phases or different timings.

Claim 15 (previously added): A voltage generating/transferring circuit according to claim 11, wherein gate and source voltage levels of said first transistor gradually rise while changing in opposite phases.

Claim 16 (previously added): A voltage generating/transferring circuit according to claim 11, further comprising:

a circuit for fixing the gate of said first transistor to low level in an OFF state.

Claim 17 (previously added): A voltage generating/transferring circuit according to claim 11, wherein a threshold voltage of the second transistor in at least one of the boost units is lower than a threshold voltage of said first transistor.

Claim 18 (previously added): A voltage generating/transferring circuit according to claim 17, wherein a transistor having a threshold voltage lower than the threshold voltage of said first transistor is arranged in a boost unit closest to the output node.

Claim 19 (previously added): A voltage generating/transferring circuit according to claim 11, wherein a threshold voltage of a transistor in a boost unit on the output node side is lower than a threshold voltage of a transistor in a boost unit on the input node side.

Claim 20 (previously added): A voltage generating/transferring circuit according to claim 11, further comprising:

a third transistor which has a gate connected to the output node, and transfers a third voltage,

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wherein a second voltage of the gate of said third transistor is equal to, or larger than a

sum of the third voltage and a threshold voltage of said third transistor in transferring the third

voltage.

Claim 21 (previously amended): A voltage generating/transferring circuit comprising:

a boost unit group including at least a first boost unit and a second boost unit series-

connected between input and output nodes;

a first transistor connected between the input node and a node for receiving a first

voltage; and

a first capacitor having one end which is connected to the output node, and another end

which receives a first oscillation signal,

wherein each of said first and second boost units has an input portion, an output portion, a

second transistor having both a gate and drain connected to the input portion and a source

connected to the output portion, and a second capacitor in each of said first and second boost

units connected to the input portion, the source of the second transistor of said first boost unit

being directly connected to the input portion of said second boost unit, and a gate of said first

transistor being connected to the input portion of one of said first and second boost units.

Claim 22 (previously added): A voltage generating/transferring circuit of claim 21, wherein the

gate of said first transistor is directly connected to the input portion of one of said first and

second boost units.

Claim 23 (previously added): A voltage generating/transferring circuit according to claim 1,

wherein the first oscillation signal and an oscillation signal which is input to the boost unit

connected to the first capacitor have opposite phases or different timings.

Claim 24 (previously added): A voltage generating/transferring circuit according to claim 11,

wherein the first oscillation signal and an oscillation signal which is input to the boost unit

connected to the first capacitor have opposite phases or different timings.

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Claim 25 (new): A voltage generating/transferring circuit according to claim 1, wherein a threshold voltage of the second transistor is lower than a threshold voltage of the first transistor.

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Claim 26 (new): A voltage generating/transferring circuit according to claim 11, wherein a threshold voltage of the second transistor is lower than a threshold voltage of the first transistor.

Claim 27 (new): A voltage generating/transferring circuit according to claim 21, wherein a threshold voltage of the second transistor is lower than a threshold voltage of the first transistor.